

WHAT IS CLAIMED:

1. A method of forming a channel region between isolation regions of an integrated circuit substrate, the method comprising:

- 5        forming a mask on the isolation region that extends onto a portion of the substrate adjacent to the isolation region to provide a shielded portion of the substrate adjacent to the isolation region and an exposed portion of the substrate spaced apart from the isolation region having the shielded portion therebetween; and  
      forming a channel region in the exposed portion of the substrate.

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2. A method according to Claim 1 wherein the forming the channel region comprises:

      implanting a first level of ions in the shielded region adjacent to the isolation region; and

- 15        implanting a second level of ions in the channel region spaced apart from the isolation region, wherein the second level is greater than the first level.

3. A method according to Claim 1 wherein the forming a channel region comprises:

- 20        implanting boron ions in the exposed region; and then  
      implanting boron difluoride ions in the exposed region.

4. A method according to Claim 1 further comprising:

- forming a gate electrode on the channel region;  
25        forming a contact on the shielded region; and  
      forming source and drain regions in the channel region self aligned to the gate electrode.

5. An integrated circuit comprising:

- 30        a substrate having an isolation region therein;  
      a channel region in the substrate having a first portion adjacent to the isolation region having a first level of ions therein and having a second portion spaced apart

from the isolation region and having the first portion therebetween, the second portion having a second level of ions therein.

- 5           6.       An integrated circuit according to Claim 5 further comprising:  
a gate electrode on the second portion;  
a contact on the first portion; and  
source and drain regions on the channel region self aligned to the gate electrode.
- 10           7.       A method of manufacturing a integrated circuit memory device, comprising the steps of:  
defining an active region comprising a first portion where a gate electrode is formed, a second portion where a bit line contact is formed, and a third portion where a storage node contact of a capacitor is formed on a integrated circuit substrate; and  
15           ion-implanting a dopant of a first conductive type into the active region on the integrated circuit substrate using a mask pattern exposing only the first and second portions of the active region as an ion-implantation mask, thereby forming a channel ion-implantation region in only the first and second portions.
- 20           8.       A method according to Claim 7 wherein the first portion comprises two regions, wherein the second portion is located between the two regions, allowing gate electrodes to be formed adjacent to both sides of the second portion.
- 25           9.       A method according to Claim 7 wherein the mask pattern is formed of a photoresist film.
10.       A method according to Claim 7 wherein the first conductive type is a p-type.
- 30           11.       A method according to Claim 7 further comprising:  
forming a gate electrode on the first portion of the active region;  
forming first and second source/drain regions in the second and third portions of the active region, respectively, using ion-implanting of a dopant of a second

conductive type opposite to the first conductive type into the second and third portions; and

forming a first contact plug self-aligned to the gate electrode and connected to the first source/drain region and forming a second contact plug self-aligned to the gate  
5 electrode and connected to the second source/drain region.

12. A method according to Claim 11 wherein the first portion comprises two adjacent regions having the second portion therebetween, wherein gate electrodes are formed on the two adjacent regions.

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13. A method according to Claim 12 wherein the first contact plug connects the first source/drain region to a bit line.

14. A method according to Claim 12 wherein the third portion in the active  
15 region comprises two regions on opposite sides of the second portion at the outside of the two regions of the first portion.

15. A method according to Claim 14 wherein the second contact plug connects the second source/drain region in the third portion to a storage node of a  
20 capacitor.

16. A method according to Claim 11 wherein the second conductive type is an n-type.